AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-2 (cancelled)

3. (currently amended) A semiconductor data processor comprising:

a first memory constituting a cache memory;

a second memory which can be used to provide a cacheable area or a non-cacheable area for the first memory; and

a read buffer which performs an operation to output data corresponding to a read access when the second memory is read accessed for the non-cacheable area;

wherein the read buffer temporarily holds predetermined access data and address data when the second memory is accessed for the non-cacheable area, [[; and]]

wherein the read buffer is connected to a first bus upstream therefrom in a transmission path of a read request and is connected to a second bus downstream therefrom in the transmission path of the read request, and

wherein the second bus ~~can transmit~~ transmits data in a first number of parallel access data bits which is ~~equal to or~~ larger than a second number of parallel access data bits [[in]] on the first bus.

4. (currently amended) The semiconductor data processor according to claim 3, wherein the read buffer includes a data register to hold read data to be transmitted through the ~~second~~ first bus, an address register to hold an address of the read data, and a control circuit to control ~~cause~~ the first bus to output the read data of the data register for a read request of an address which is coincident with the address of the read data held in the address register.

5. (cancelled)

6. (currently amended) ~~The~~ A semiconductor data processor ~~according to claim 5,~~ comprising:

a first memory constituting a cache memory;

a second memory which provides a cacheable area or a non-cacheable area for the first memory;

a read buffer which performs an operation to output data corresponding to a read access when the second memory is read accessed for the non-cacheable area;

a first bus connected between the first memory and the read buffer;

a second bus connected between the read buffer and the second memory; and

~~further comprising~~ a third bus ~~which connects~~ connected between the first memory to the second memory, in a path different from a path formed by the first and second buses, ~~when~~ to access the second memory ~~is accessed~~ for the cacheable area,

wherein the read buffer temporarily holds predetermined access data and address data when the second memory is accessed for the non-cacheable area, and

wherein a first bus and a second bus which are dedicated sequential access buses for the read buffer.

7. (currently amended) The semiconductor data processor according to claim 6, ~~wherein~~ further comprising a peripheral bus interface controller ~~is~~ connected to the third bus.

8. (original) The semiconductor data processor according to claim 6, further comprising an internal memory controller connected to the second bus and the third bus and serving to carry out an access interface control for the second memory.

9. (currently amended) The semiconductor data processor according to claim 8, wherein the third bus is provided with a secondary cache memory controller ~~to control~~ which controls the second memory as a secondary cache memory for the first memory.

10. (previously presented) The semiconductor data processor according to claim 9, wherein the secondary cache memory controller invalidates the second memory in response to a signal indicative of a cache invalidation of the first memory.

11. (previously presented) The semiconductor data processor according to claim 9, further comprising a control register which sets the internal memory controller and the secondary cache memory controller to operate exclusively of each other.

Claims 12-16 (cancelled)

17. (previously presented) A semiconductor data processor comprising:

a first memory constituting a cache memory;

a second memory which can be used to provide a secondary cache memory or memory which is not cache memory for the first memory;

a designator which selectively designates an area of the second memory as secondary cache memory or memory which is not cache memory;

a secondary cache memory controller which performs an access interface control to the second memory area as secondary cache memory;

an internal memory controller which performs access interface control to the second memory area as memory which is not cache memory; and

a read buffer which performs an operation to output data, read from the second memory area via the internal memory controller, when the second memory area is read accessed as memory which is not cache memory by the internal memory controller.

18. (currently amended) The semiconductor data processor according to claim 17, wherein the read buffer newly holds data and ~~an~~ address information corresponding to an access if it does not retain data corresponding to the access when the second memory area is accessed as memory which is not cache memory by the internal memory controller.

19. (previously presented) The semiconductor data processor according to claim 18, wherein the read buffer is connected to a first bus upstream therefrom in a transmission path of a read request and is connected to a second bus, having a greater bus width than a width of the first bus, downstream therefrom in the transmission path of the read request.